Remarks

Claims 1, 2, 6-11, 13-15, 18 and 19 are pending in the present application. Claims 1, 2, 6-11, 13-15, 18 and 19 have all been rejected under 35 U.S.C. § 102(b) as being anticipated by Crampton. In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1, 2, 6-11, 13-15, 18 and 19 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Crampton (U.S. Pat. No. 5,767,721). For the reasons set forth below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

The present invention comprises, in one exemplary embodiment, a switch 40 including a series switching transistor 42 and a shunt transistor 46 (See Fig. 3). A signal path 51 couples a radiofrequency (RF) input port 12 to an RF output port 14. A first control voltage V_{HI} is coupled to the signal path 51 near the input port 12. A second control voltage V is coupled to the series switching transistor 42 at its gate, and to the shunt transistor 46.

Importantly, a drain terminal of the shunt transistor 46 is directly coupled to a gate terminal of the series switching transistor 42. This direct coupling of the transistors 42 and 46 allows the same control signal (i.e., control voltage "V") to have the opposite effect on each transistor (i.e., turning one ON when the other is OFF, and vice versa), and to thus permit a common logic signal to control both transistors (see, page 7, Paragraphs [0029], [0030] of the specification). This direct coupling also eliminates the need for a complex system of bias

resistors, as exist in some prior art circuits (e.g., Crampton, discussed below).

Independent claim 1 now recites:

> An integrated circuit switch comprising: at least two signal ports coupled by a signal path, the signal path including a channel of at least one series FET; a shunt path coupled to ground and including a channel of a shunt FET; a first control voltage applied to the signal path; and, a second control voltage applied to a gate of the series FET and to a drain/source of the shunt FET, wherein a drain terminal of the shunt FET is directly coupled to a gate terminal of the series FET [emphasis added].

Thus, claim 1 requires a switch circuit including a "shunt FET" with its drain terminal directly coupled to the gate terminal of a "series FET." Crampton fails to disclose, teach or suggest such an invention.

Crampton teaches a switch circuit 56 with an RF input 58 and an RF output 70. The switch circuit 56 also includes depletion mode FETs 64, 80 which are coupled to a control voltage V1. Crampton does not disclose, teach or suggest a drain terminal of the (shunt) FET 80 being directly coupled to a gate terminal of the (series) FET 64.

In fact, the drain terminal of FET 80 is connected to the gate of FET 64 through a network of large resistance value biasing resistors 72, 76. Crampton teaches that these biasing resistors 72, 76 should "each have a large resistance value of at least 50 Kilohms" (see, col. 4 lines 30-33). As explained in Crampton, the biasing resistors 72 and 76 are necessary for the proper operation of the circuit. In particular, biasing resistor 72 enables FET 64 to "be turned off when V_1 is at a zero potential" (see, col. 4, lines 12-15). Similarly, biasing resistor 76 enables FET 80 to "be turned on when V_1 is at a zero voltage and turned off when V_+ is at a significant positive voltage" (see, col. 4, lines 25-35). By directly coupling the drain of transistor 46 to the

gate of transistor 42, the Applicant of the present invention has eliminated the need for a complex network of biasing resistors, such as resistors 72 and 76 in Crampton.

In sum, Crampton fails to disclose, teach or suggest a switch circuit including a "shunt FET" with its drain terminal directly coupled to the gate terminal of a "series FET." Thus, reconsideration and withdrawal of this ground of rejection with respect to independent claim 1, is respectfully requested.

Independent claims 2, 6, 8 and 9 have been amended to include similar limitations to those discussed above with reference to claim 1. Therefore, for at least those reasons discussed above with respect to claim 1, reconsideration and withdrawal of this rejection with respect to claims 2, 6-11, 13-15, 18 and 19 is also respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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